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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,029	09/12/2003	Jyh Chain Lin		9296

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EXAMINER	
ALMO, KHAREEM E	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/662,029	LIN, JYH CHAIN	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/12/2003; 6/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 objected to because of the following informalities: With respect to claim 8 lines 11 and 12 fails to distinguish which amplifier "the amplifier" refers to. (i.e. Is it the first operational amplifier or the second operational amplifier.). Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by AAPA.

With respect to claim 1, figure 4 of Applicant's admitted Prior Art discloses a pulse width modulation current adjustment apparatus comprising: a triangle wave generator (1) for generating a triangle wave signal; a comparator (2), a field effect transistor (3), a power supply (7), a first resistor (4), and a second resistor (5); wherein the triangle wave signal and a modulation signal are input to the comparator, and an output of the comparator is connected to a gate terminal of the FET, the first resistor is connected between the power supply (7) and a source terminals (S) of the FET, and a

drain terminal (D) of the FET outputs a driving current through the second resistor (5) to a load.

With respect to claim 2, figures 4 and 5 of AAPA disclose a pulse width modulation current adjustment apparatus as described in claim 1, wherein the triangle wave signal is a symmetric triangle wave signal (i.e. the individual triangles within each period form a perfect isosceles triangle with the base being the leftmost rising edge and the sides being the period and the right edge.)

With respect to claim 7, figure 4 of AAPA discloses a circuit in which the recited method of making a pulse width modulation current adjustment apparatus comprising the steps of: providing a triangle wave generator for generating a triangle wave signal, connecting a comparator to said triangle wave generator, connecting a voltage source to said comparator; connecting said comparator to a gate terminal of a field effect transistor; connecting a power supply to a source terminal via a first resistor and connecting a load to a drain terminal of the FET via a second resistor is inherent.

With respect to claim 8, figure 6 of AAPA, discloses a triangle wave generator for use with a pulse width modulation current adjustment apparatus comprising a first operational amplifier (); a front resistor (connected to ground) electrically connecting a negative terminal of the amplifier (between R1 and D1) and ground; a first feedback resistor (R4) a second feedback resistor (R2) and a current limiting resistor ((connected to positive terminal of first operational amplifier) so as to form a zero-crossing comparator, a second operational amplifier (connected to uo) a current limiting resistor (R3) and a capacitor (C) together forming an integrator; a back grounding resistor (R1

grounded through Uz) electrically connected to a positive terminal of the amplifier (between R1 and D1) to ground; and an output of the first operational amplifier (between R1 and D1) electrically connected to said positive terminal via said current limiting resistor (R4) and an output of the second operational amplifier (connected to uo) electrically connected to the positive terminal of the second operational amplifier and also electrically connected to the positive terminal of the first operational amplifier via the second feedback transistor (R2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 4 of AAPA.

With respect to claims 3-6, figure 4 discloses a pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is an N-channel type FET. It would be obvious to one skilled in the art at the time the invention was made to interchange different types of FET transistors for the purpose of optimizing the circuit to work in different environments. (i.e. to switch on a high signal, low signal etc.)

6. Claims 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haas (US 3621282).

With respect to claims 1, and 3-6, figure 4 of (US 3621282) discloses a pulse width modulation current adjustment apparatus comprising: a triangle wave generator for generating a triangle wave signal (SAWTOOTH OUTPUT); a comparator (COMPARATOR), a transistor (Q1), a power supply (+12V or –6V), a first resistor (R4), and a second resistor (between Q1 and Q2); wherein the triangle wave signal and a modulation signal are input to the comparator, and an output of the comparator is connected to a gate terminal of the transistor, the first resistor is connected between the power supply (+12V) and a terminal of the transistor, and a terminal of the transistor outputs a driving current through the second resistor to a load, but fails to disclose wherein the transistor is a FET. It would be obvious at the time the invention was made to a person having ordinary skill in the art to use any FET in place of the BJT for the purpose of more stable switching.

With respect to claim 7, the circuit above produces a circuit in which the recited method of making a pulse width modulation current adjustment apparatus comprising the steps of : providing a triangle wave generator for generating a triangle wave signal, connecting a comparator to said triangle wave generator, connecting a voltage source to said comparator; connecting said comparator to a gate terminal of a field effect transistor; connecting a power supply to a source terminal via a first resistor and connecting a load to a drain terminal of the FET via a second resistor is inherent.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
12/18/2006

Quan Tra
PRIMARY EXAMINER